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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,547	12/21/2001	Alok Jain	15448-0505	4676
29989	7590	08/10/2005	EXAMINER	
HICKMAN PALERMO TRUONG & BECKER, LLP 2055 GATEWAY PLACE SUITE 550 SAN JOSE, CA 95110			JONES, HUGH M	
			ART UNIT	PAPER NUMBER
			2128	
DATE MAILED: 08/10/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/029,547	JAIN ET AL.
	Examiner	Art Unit
	Hugh Jones	2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 21 December 2001.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-39 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 21 December 2001 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/11/2002.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

1. Claims 1-39 of U. S. Application 10/029,547 filed 12/21/2001, are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
4. Claims 1-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer ("K") in view of Allred ("A").
5. Kramer discloses that FETs can be used as memory cells (# 10, fig. 2), including their use in memory arrays (# 42, fig. 4).
6. Kramer does not disclose functional abstraction of the memory array.
7. Allred discloses functional abstraction of FET circuits (specifics provided below).
8. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Kramer disclosure with the Allred teaching for the following

reasons. It is cheaper and more efficient to model circuits before manufacturing them in order to avoid faulty circuit design; Allred disclose (col. 1) that functional abstraction is used to model FET circuits.

9. Specifically, the applied art discloses:

A computer implemented method for functionally abstracting a memory column, comprising

identifying, in a description of a circuit, at least one column of n memory cells, where n is an integer greater than 1 (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET);

representing said column of n memory cells as a single-memory-cell column comprising a single representative memory cell (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET);

abstracting at least a portion of said single-memory-cell column to derive a logic-level representation for said representative memory cell (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET); and

generating one or more additional instances of said logic-level representation to

derive an abstracted memory column comprising a plurality of instances of said logic-level representation (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

wherein said logic-level representation comprises a latch (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

wherein generating one or more additional instances comprises: generating n-l additional instances of said logic-level representation to derive an abstracted memory column comprising n instances of said logic-level representation (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

deriving a gate-level representation for said representative memory cell (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET); and

abstracting a latch from at least a portion of said gate-level representation (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of

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memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

applying symbolic analysis to a transistor level description of said representative memory cell (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

verifying that all of said n memory cells are substantially identical in structure relative to each other (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

selecting one of said n memory cells to be said representative memory cell (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

removing all of said n memory cells except for said representative memory cell from said column (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

wherein said representative memory cell is initially coupled to a particular select line (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET), and wherein representing said column of n memory cells as a single-memory cell column comprises;

decoupling said representative memory cell from said particular select line (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

coupling said logic-level representation of said representative memory cell to said particular select line (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

generating one or more additional instances of said logic-level representation (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET); and for each additional instance generated, coupling that instance to a distinct select making an explicit assumption that selection of each select line is mutually exclusive relative to all other select lines (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an

array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

wherein said abstracted memory column is cycle ready (K: FET is a memory cell - fig. 2, fig. 4 #42 memory structure is an array of columns of memory cells; A: col. 1 – functional abstraction, col. 6, line 66 to col. 7, line 52 functional abstraction and replacing multiple parallel connected FETs with a single FET).

10. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to: Dr. Hugh Jones telephone number (571) 272-3781,

Monday-Thursday 0830 to 0700 ET,

or

the examiner's supervisor, Jean Homere, telephone number (571) 272-3780.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)

or (703) 308-1396 (for informal or draft communications, please label *PROPOSED* or *DRAFT*).

Dr. Hugh Jones
Primary Patent Examiner

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July 23, 2005

Hugh Jones, Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100